REMARKS

Claims 1-10 are cancelled without prejudice or disclaimer. New claims 11-19 are added. Therefore, claims 11-19 are the claims currently pending in the Application.

Objections

The Examiner objects to page 2, lines 2-3, and directs that all references to "simulation platform" be changed to "simulation program" in the Specification and the Abstract. The Examiner objects to page 2, lines 24-25. The Examiner objects to page 11, lines 19-20, on the ground that the cited lines contain a typographical error.

The Specification and Abstract are amended. Therefore these objections should now be withdrawn.

Claims 1-10 are objected to based on various informalities cited. Claims 1-10 are cancelled without prejudice or disclaimer, therefore this objection is moot.

Rejection of Claims 1-10 under 35 U.S.C. § 1.112, First Paragraph

Claims 1-10 are rejected under 35 U.S.C. § 1.112, first paragraph, on the ground that they contain subject matter that was not described in the Specification in such a way as to reasonably convey to one skilled in the art that the inventors had intellectual possession of the claimed invention.

Claims 1-10 are cancelled without prejudice or disclaimer, and this rejection is therefore moot. Accordingly, this rejection should now be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1, 4 and 9 are rejected under 35 U.S.C. § 103 as being obvious from Chang et al. U.S. Patent 6, 269,467, and Tseng et al., U.S. Patent 6,321,366 in view of Swoboda et al. U.S. Patent No. 6,546,505. Claims 2 and 3 are rejected under 35 U.S.C. § 103

as being obvious from Chang, Tseng, Swoboda in view of Dangelo et al U.S. Patent No. 5,801,958. Further claims 5 and 6 are rejected under 35 U.S.C. § 103 as being obvious from Chang, Tseng, Swoboda and Fujiwara.

Claims 1-6 and 9 are cancelled without prejudice or disclaimer. Therefore, this rejection is moot, and should now be withdrawn.

Claims 11-19 do not introduce impermissible new matter. Claims 11-19 are fully supported by the Specification. For instance, as explained on page 4, lines 1-13, according to an aspect of Applicant's claimed invention, an improvement for the design and development for LSI is provided, such that sources or elements representing hardware and other sources or elements representing software described by a general purpose high-level language are designed and evaluated by counting traffic of a software bus interconnecting the sources or elements representing the hardware and the software.

By way of background information, in Ernst, R., Henkel, J., Beuner, I. "Hardware-Software Co-Synthesis for Microcontrollers", IEEE Design and Test of Computers, IEEE Computers Society, Los Alamitos, US (01-12-1993), 10 (4), 64-65-75, a software oriented approach to hardware-software partitioning is presented, which avoids restrictions on the software semantics. Furthermore, an interactive partitioning process based hardware extraction" is disclosed which is controlled by a cost function. This process is used in COSYMA, an experimental co-synthesis system for embedded controllers. The co-synthesis is based on the standard micro controller architecture, consisting of a processor core, memory, and customized hardware. The system description used in the co-synthesis system is input in C language and translated into an internal graph representation suitable for partitioning. The hardware-software partitioning is done by marking nodes of the graph to be

moved to hardware. A translator generates C functions for the software. Then, the hardware-software communication protocol is inserted. A standard C compiler generates the object code, which can then be simulated with an RT-level simulator. Then, a run-time analysis on the object code is executed to check for violations of the timing constrains in the C description. This runtime analysis can be an RT-level simulation, and hence its carried out on a low-level design stage.

Further, in Drach, N., Tmam, 0., "Software Assistance for Data Caches", Future Generations Computer Systems, Elsevier Sience Publishers, Amsterdam. NL (01-10-1995), 11(6), 519-536, a method on hardware and software cache optimizations is disclosed and the performance of combined through simple software hardware optimizations is investigated. Because current caches provide little flexibility for exploiting temporal and spatial locality, two hardware modifications are proposed to support these two kinds of locality. Spatial locality is exploited by using large physical cache lines which do not exhibit the performance flows of large physical cache lines. Temporal locality is exploited by minimizing cache pollution with a bypass mechanism that still allows to exploit spatial locality. Subsequently, it is shown that simple software information on the spatial *I* temporal locality of array references, as provided by current locality optimization algorithms, can be used to increase cache performance significantly.

In Hermann, D., Henkel, I, and Ernst, R.: "An "Approach to the Adaption of estimated Cost Parameters in the COSYMA-System", hardware/software co-design, 1994, proceedings of the third international workshop on ..., Grenoble, France, 22-24 September 1994, Los Alamitos, US, IEEE Computer Society (22-09-1994), 100-

107, a hardware/software partitioning method used in hardware/software co-design is disclosed by using the COSYMA-system. The system uses simulated annealing based on estimated costs. Deviations between estimated and real costs seem unavoidable due to synthesis, compiler and communication effects. An approach to adapt these estimations is disclosed which shows fast conversions of estimated to real costs.

In COSYMA architecture and input languages (15-10-1998), httpi/www.ida.ing.tubs.de/researchlprojects/cosymaloverview/note2.html, the COSYMA-system is presented as a platform for exploration of the co-synthesis process.

For at least the reasons set forth in the foregoing discussion, Applicant believes that the Application is now allowable, and respectfully requests that the Examiner reconsider the rejections and allow the Application. Should the Examiner have any questions regarding this Amendment, or regarding the Application generally, the Examiner is invited to telephone the undersigned attorney.

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